**COA MCQ CHAPTER 4**

Q1. LRU stands for \_\_\_\_\_\_\_\_.

1. Low Rate Usage
2. Least Rate Usage
3. Least Recently Used
4. Low Required Usage

ANS 1. C

Q2. When the data at a location in cache is different from the data in the main memory, the cache is called \_\_\_\_\_\_\_\_\_\_.

1. Unique
2. Inconsistent
3. Variable
4. Fault

ANS 2. B

Q3. Which of the following is not a write policy to avoid Cache Coherence?

1. Write through
2. Write within
3. Write back
4. Write buffer

ANS 3. B

Q4. In \_\_\_\_\_\_\_\_\_\_\_ mapping, the data can be mapped anywhere in the Cache Memory.

1. Associative
2. Direct
3. Set-associative
4. Indirect

ANS 4. A

Q5. To get the physical address from the logical address generated by CPU we use \_\_\_\_\_\_\_\_

1. MAR
2. MMU
3. Overlays
4. TLB

ANS 5. B

Q6. During the transfer of data between the processor and memory we use \_\_\_\_\_\_\_\_.

1. Cache
2. TLB
3. Buffers
4. Registers

ANS 6. D

Q7. \_\_\_\_\_\_\_ method is used to map logical address of variable length onto physical memory.

1. Paging
2. Overlays
3. Segmentation
4. Paging with segmentation

ANS1. C

Q8. Physical memory is divided into sets of finite size called as \_\_\_\_\_\_\_\_\_\_.

1. Frames
2. Pages
3. Blocks
4. Vectors

ANS1. A

Q9. What is the high speed memory between the main memory and the CPU called?

1. Registers
2. Cache memory
3. Secondary storage memory
4. Virtual memory

ANS 9. B

Q10. Whenever the data is found in the cache memory it is called a \_\_\_\_\_\_\_\_.

1. HIT
2. MISS
3. FOUND
4. ERROR

ANS 10. A

Q11. The transfer between CPU and Cache is called \_\_\_\_\_\_\_\_.

1. Block transfer
2. Word transfer
3. Set transfer
4. Associative transfer

ANS 11. B